REMARKS

The Official Action dated October 6, 2003 has been carefully considered. Accordingly, the changes presented herewith, taken with the following remarks, are believed sufficient to place the present application in condition for allowance. Reconsideration is respectfully requested.

Claims 1-3, 6, 8-12, 14, 16-22, 25, 28, 30 and 32 have been amended and Claims 12, 18 and 33 has been cancelled. The amendments to the claims were to correct minor informalities. In addition claim 10 was amended to incorporate the limitations of original claim 12, and claim 16 was amended to incorporate the limitations of original claim 18. Support for the amended claims may be found in original claims. Since these changes do not involve any introduction of new matter, entry is believed to be in order and is respectfully requested.

In the Official Action, the Examiner asserted the title was not descriptive. The present amendment amends the title to a more descriptive title. Reconsideration is respectfully requested.

In the Official Action, the Examiner objected to the abstract of the disclosure as not covering a full description of the technical disclosure was not descriptive. The present amendment amends the abstract to more fully describe the entire claimed invention and technical disclosure. Reconsideration is respectfully requested.

In the Official Action, the Examiner objected to Figures 1-5, 6A, 6C, 8A, 9-10, 11A, and 13-14. A Request For Authorization To Amend Drawings is submitted with this Amendment under separate letter in compliance with MPEP § 608.02 (r). If the proposed drawing corrections are accepted by the Examiner, Applicant will then forward Formal Drawings reflecting the accepted changes to the drawings. Reconsideration is respectfully requested.

In the Official Action, claims 14, 19, 20, 25-28 and 31-33 were rejected under 35 U.S.C § 112, second paragraph as being indefinite. Claims 14, 19, 28 and 32 have been amended to more clearly point and distinctly claim the subject matter of the present invention. Claim 33 has been cancelled. Whereby, it is believed the Examiner's rejection has been overcome. Reconsideration is respectfully requested.

In the Official Action, claims 1-37 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-9 of U.S. Patent No. 6,546,438 (Note: The Examiner's Official Action listed U.S. Patent No. 6,546,348, Applicants believe this was a typographical error and was intended to be U.S. Patent No. 6,546,438 and the following remarks are directed to such). While Applicants believe the present claims are patentably distinguishable from the '438 patent claims, Applicants submit with this Amendment a Terminal Disclaimer in compliance with 37 C.F.R. 1.321(c) to overcome the rejection based on the non-statutory double patenting. The filing of a Terminal Disclaimer simply serves as a statutory function of removing the rejection of double patenting and raises neither presumption nor estoppel on the merits of the rejection, *Quad Environmental Technology v. Union Sanitary District*, 20 U.S.P.Q.2d 1392 (Fed. Cir. 1991). Accordingly, the rejection has been overcome. Reconsideration is respectfully requested.

In the Official Action, claims 10-12, 14-18, 21-24, 29-30 and 36-37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art in view of Kobayashi (US Patent No. 6,199,122) and Noll (US Patent No. 5,544,334) taken together. The Examiner asserted that the applicants' admitted prior art discloses various methods for writing and reading to and from storage devices were well known at the time the invention was made. The Examiner asserted that Kobayashi disclose various methods for reading and writing data to and from devices such as hard drive controllers and storage devices, and the Examiner further asserted that Kobayashi teaches converting between a serial stream or

standard and a parallel standard or protocol. The Examiner asserted Noll discloses methods for reading and writing between devices utilizing different industry standards or protocols. The Examiner further asserted that Noll discloses the use of a memory or buffer in an interface so as to provide different data rates between different devices or standards. The Examiner asserted one of ordinary skill in the art would have found it obvious to provide an interface and convert between a serial stream or standard and a parallel stream or protocol in a system having a controller utilizing serial data streams in order to provide compatibility with a large number of industry standard devices.

However, as will be set forth in detail below, it is submitted that the methods of claims 10-12, 14-18, 21-24, 29-30 and 36-37 are non-obvious over and patentably distinguishable from the teachings of applicants' admitted prior art in view of Kobayashi and Noll. Accordingly, this rejection is traversed and reconsideration is respectfully requested.

As defined by claim 10, the present invention is directed to a method for writing a serial data stream to a component associated with parallel data streams.. The method comprises: receiving the serial data stream; converting the serial data stream to a parallel data stream; loading the parallel data stream converted from the serial data stream in memory; and writing the parallel data stream from the memory to the component; wherein the step of converting the serial data stream to a parallel data stream comprises the steps of: synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the data shifted out of the register comprises the parallel data stream loaded in the memory.

Applicants' admitted prior art discloses that hard disk drives in the mid-1980's often utilized electrical interfaces compliant with the IEEE 412 standard. In the early 1990's, ATA disk drive interface standard became popular and the IEEE 412 technology became obsolete and as such replacement parts have been difficult to find for IEEE 412 standard dependent

devices. Kobayashi discloses a computer system and medium for converting a serial command and data standard to a parallel one. Kobayashi discloses converting from a Universal Serial Bus (USB) standard to the ATA standard to allow compatibility with existing memory devices. Noll discloses an interface which allows an integrated device electronics (IDE) disk storage device to connect to a Micro Channel bus.

References relied upon to support a rejection under 35 U.S.C. §103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. *In re Payne* , 203 U.S.P.Q. 245 (C.C.P.A. 1979). Applicants find no teaching by applicants' admitted prior art, Kobayashi or Noll, alone or in combination, of a method for writing a serial data stream to a component associated with parallel data streams comprising, *inter alia*, the step of converting the serial data stream to a parallel data stream, which comprises the steps of: synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the data shifted out of the register comprises the parallel data stream loaded in the memory. Since none of the references relied upon by the Examiner disclose or suggest that concept, there is no way the references could be combined to meet the limitations of Applicants claims.

Furthermore, to establish prima facie obviousness of the claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). In view of the failure of applicants' admitted prior art, Kobayashi or Noll, alone or in combination, to teach, disclose or suggest a method writing a serial data stream to a component associated with parallel data streams comprising, *inter alia,* the step of converting the serial data stream to a parallel data stream, which comprises the steps of: synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the

data shifted out of the register comprises the parallel data stream loaded in the memory, applicants' admitted prior art, Kobayashi and Noll do not render the presently claimed methods for writing a serial data stream to a component associated with parallel data streams obvious.

As defined by claim 16, the present invention is directed to a method for reading a serial data stream from a component associated with parallel data streams. The method comprises receiving a request for data associated with the component; receiving a parallel data stream from memory in response to the request for data; converting the received parallel data stream to the serial data stream; and outputting the serial data stream; wherein the step of converting the received parallel data stream to the serial data stream comprises the steps of: shifting the received parallel data stream into a parallel-to-serial register; and shifting the serial data stream out of the register.

As noted above, references relied upon to support a rejection under 35 U.S.C. §103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. *In re Payne , supra.* Applicants find no teaching by applicants' admitted prior art, Kobayashi or Noll, alone or in combination, of a method for reading a serial data stream from a component associated with parallel data streams comprising, *inter alia*, the step of converting the received parallel data stream to the serial data stream, which comprises the steps of: shifting the received parallel data stream into a parallel-to-serial register; and shifting the serial data stream out of the register. Since none of the references relied upon by the Examiner disclose or suggest that concept, there is no way the references could be combined to meet the limitations of Applicants claims.

Furthermore, to establish prima facie obviousness of the claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka, supra.* In view of the failure of applicants' admitted prior art, Kobayashi or Noll, alone or in combination, to teach, disclose or suggest a method for reading a serial data stream from a component associated with parallel data streams comprising, *inter alia*, the step of converting the received parallel data stream to the serial data stream, which comprises the steps of: shifting the received parallel data stream into a parallel-to-serial register; and shifting the serial data stream out of the register, applicants' admitted prior art, Kobayashi and Noll do not render the presently claimed methods for reading a serial data stream from a component associated with parallel data streams obvious.

It is therefore submitted that the presently claimed methods are non-obvious over and patentably distinguishable from applicants' admitted prior art in view of Kobayashi and Noll, taken together. Reconsideration is respectfully requested.

Claims 13, 19-20, 25-28 and 31-33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art in view of Kobayashi and Noll, taken together and further in view of Weber et al. (US Patent No. 5,133,060). In making this rejection, the Examiner conceded that neither applicants' admitted prior art, Kobayashi or Noll teach a buffer used in conjunction with the serial to parallel and parallel to serial conversion as being a cache buffer memory. The Examiner took the position that Weber et al. teach an interface between a computer or controller including an interface using serial to parallel and parallel to serial conversion, and additionally teach a cache buffer memory in the interface to provide fast access to stored data. The Examiner asserted one of ordinary skill in the art would have found it obvious to utilize a cache buffer memory in conjunction with an interface between a disk drive and a controller.

However, as will be set forth in detail below, it is submitted that the methods of claims 13, 19-20, 25-28 and 31-33 are non-obvious over and patentably distinguishable from the teachings of applicants' admitted prior art in view of Kobayashi and Noll and in further view of Weber et al. Accordingly, this rejection is traversed and reconsideration is respectfully requested.

The teachings of applicants' admitted prior art in view of Kobayashi and Noll are disclosed above. The deficiencies of applicants' admitted prior art in view of Kobayashi and Noll are not overcome with the combination of Weber et al. Moreover, Weber et al. alone or in combination with applicants' admitted prior art, Kobayashi and Noll, fail to teach or disclose a method for writing a serial data stream to a component associated with parallel data streams comprising, *inter alia*, the step of converting the serial data stream to a parallel data stream, which comprises the steps of: synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the data shifted out of the register comprises the parallel data stream loaded in the memory.

Weber et al. teach a controller for use with a storage medium, wherein the controller provides a memory cache. The controller comprises a disk interface which provides the serial-to-parallel and parallel-to-serial conversion of the data. As required by independent claim 10 of the present invention, the method requires synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the data shifted out of the register comprises the parallel data stream loaded in the memory. In addition, as required by independent claim 16 of the present invention, the method requires shifting the received parallel data stream into a parallel-to-serial register; and shifting the serial data stream out of the register. The

controller and associated interface of Weber et al. fail to teach such capabilities as required by the present claims.

References relied upon to support a rejection under 35 U.S.C. §103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. *In re Payne, supra.* Furthermore, to establish prima facie obviousness of the claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka, supra.* In view of the failure of applicants' admitted prior art, Kobayashi, Noll and Weber et al., alone or in combination, to teach, disclose or suggest the methods for writing a serial data stream to a component associated with parallel data streams comprising, *inter alia*, the step of converting the serial data stream to a parallel data stream, which comprises the steps of: synchronizing a clock signal with the serial data stream; shifting the synchronized data stream into a serial-to-parallel register; and shifting data out of the register, wherein the data shifted out of the register comprises the parallel data stream loaded in the memory, the combination of applicants' admitted prior art, Kobayashi, Noll and Weber et al. do not support a rejection of claim 13 under 35 U.S.C. §103.

In addition, in view of the failure of applicants' admitted prior art, Kobayashi, Noll and Weber et al., alone or in combination, to teach, disclose or suggest the methods for reading a serial data stream from a component associated with parallel data streams comprising, *inter alia*, the step of converting the received parallel data stream to the serial data stream, which comprises the steps of: shifting the received parallel data stream into a parallel-to-serial register; and shifting the serial data stream out of the register, the combination of applicants' admitted prior art, Kobayashi, Noll and Weber et al. do not support a rejection of claims 19-20, 25-28 and 31-33 under 35 U.S.C. §103.

When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references. *In re Rouffet*, 149 F.3d

1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Applicant finds no teaching or suggestion for the combination of applicants' admitted prior art, Kobayashi and Noll with Weber et al. Applicants' admitted prior art discloses that hard disk drives in the mid-1980's often utilized electrical interfaces compliant with the IEEE 412 standard and later in the early 1990's, the ATA disk drive interface standard became popular and the IEEE 412 technology became obsolete. Kobayashi discloses a computer system and medium for converting a serial command and data standard to a parallel one. Kobayashi discloses converting from a Universal Serial Bus (USB) standard to the ATA standard to allow compatibility with existing memory devices. Noll discloses an interface which allows an integrated device electronics (IDE) disk storage device to connect to a Micro Channel bus. On the other hand, Weber et al. teach a controller for use with a storage medium, wherein the controller provides a memory cache. The Examiner in the Official Action asserted the suggestion for the combination of applicants' admitted prior art, Kobayashi and Noll with Weber et al. as "in order to reduce overall access times and increase operating speed, and to prevent the controller or processor from experiencing excessive idle times due to differences in transfer rates." (Page 24 of Paper Number 3).

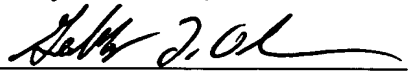
Although the suggestion to combine references may flow from the nature of the problem, "defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness," *Monarch Knitting Mach. Corp. v. Sulzer Morat Gmbh*, 139 F.3d 877, 880, 45 U.S.P.Q.2D (BNA) 1977, 1981 (Fed. Cir. 1998). Therefore, "when determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art as a whole to

suggest the desirability, and thus the obviousness, of making the combination.'" *In re Beattie*, 974 F.2d 1309, 1311-12, 24 U.S.P.Q.2D (BNA) 1040, 1042 (Fed. Cir. 1992).

It is well settled that the Examiner cannot pick and choose among individual elements of assorted prior art references to recreate the claimed invention based on the hindsight of the Applicant's invention. Rather, the Examiner has the burden to show some teaching or suggestion in the references to support the use and the particular claimed combination, as in the present invention, *Smith-Kline Diagnostics, Inc. v. Helena Laboratories Corp.*, 8 U.S.P.Q.2d 1468, 1475 (Fed. Cir. 1988). Additionally, the mere fact that it is possible to find isolated disclosures which might be combined in such a way to produce a new composition does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination, *In re Grabiak*, 226 U.S.P.Q. 870, 872 (Fed. Cir. 1985). Applicant finds no teaching or suggestion for the combination of applicants' admitted prior art, Kobayashi and Noll with Weber et al.

It is believed that the above represents a complete response to the Examiner's rejections under 35 U.S.C. §§103 and 112 and places the present application in condition for allowance. Reconsideration and an early allowance are requested.

Respectfully submitted,

By 

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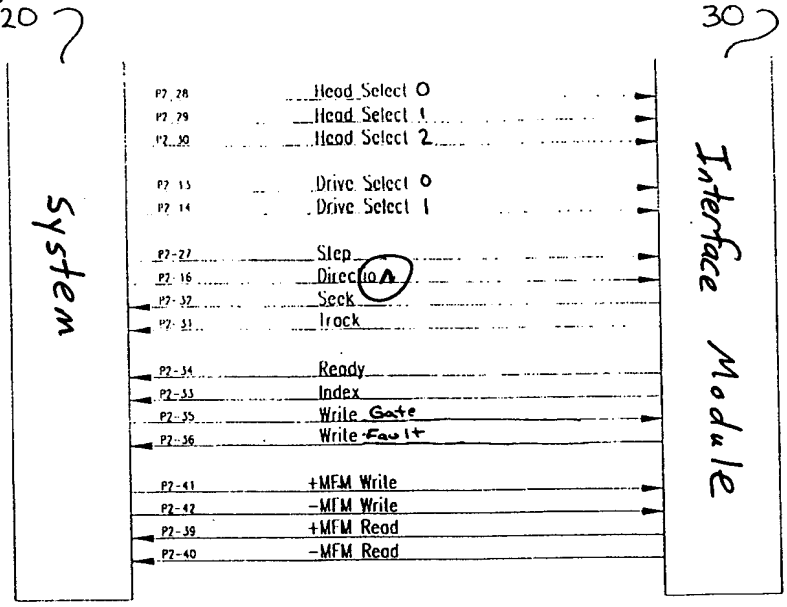

FIG. 1

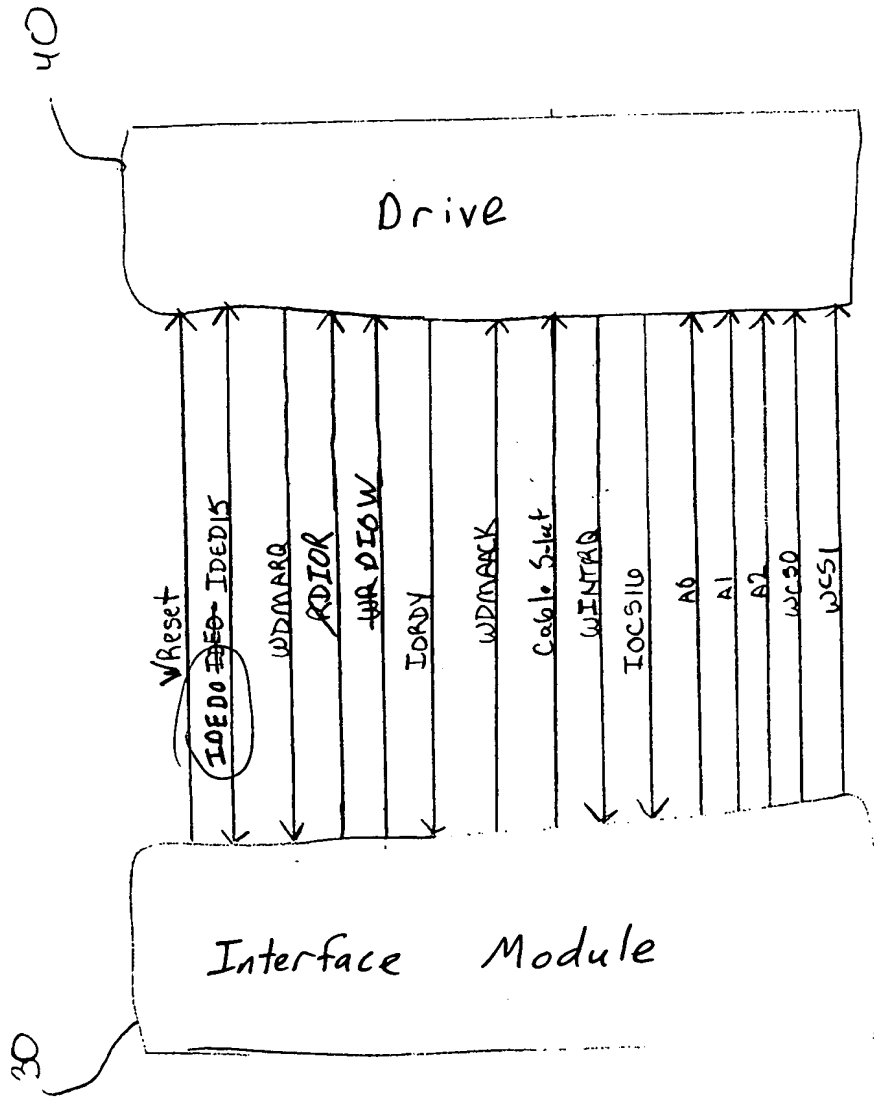

FIG. 2

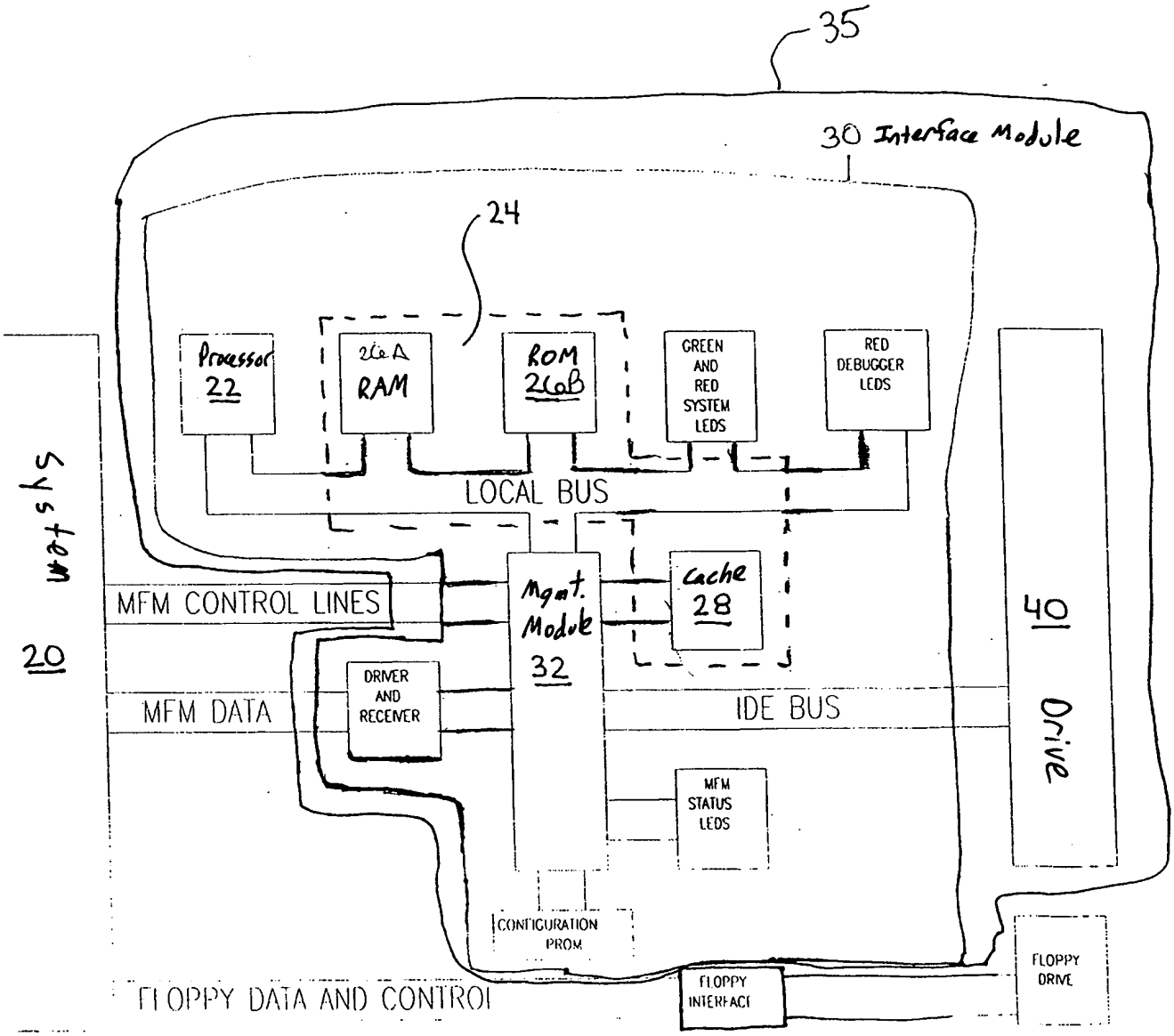

FIG. 3

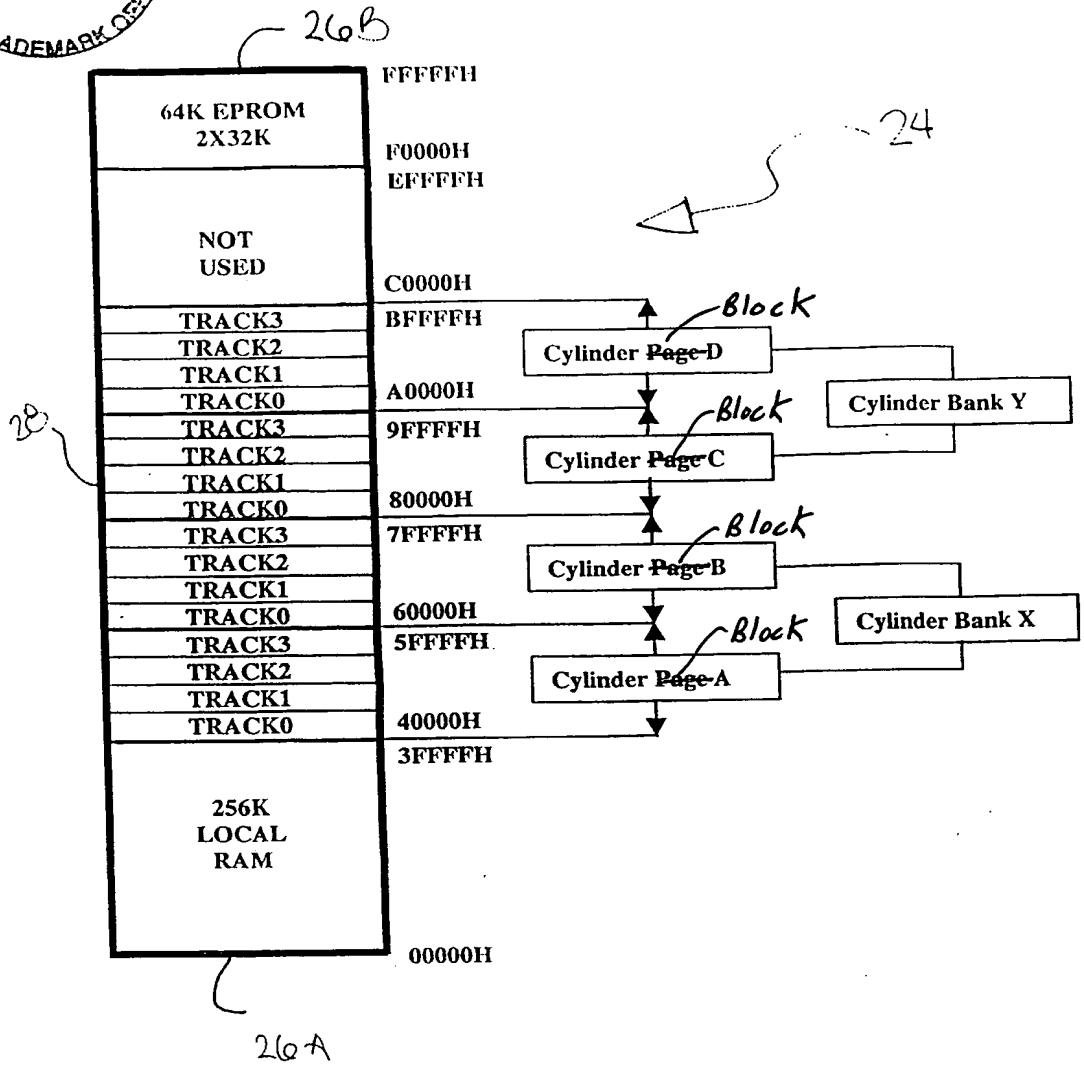

FIG. 4

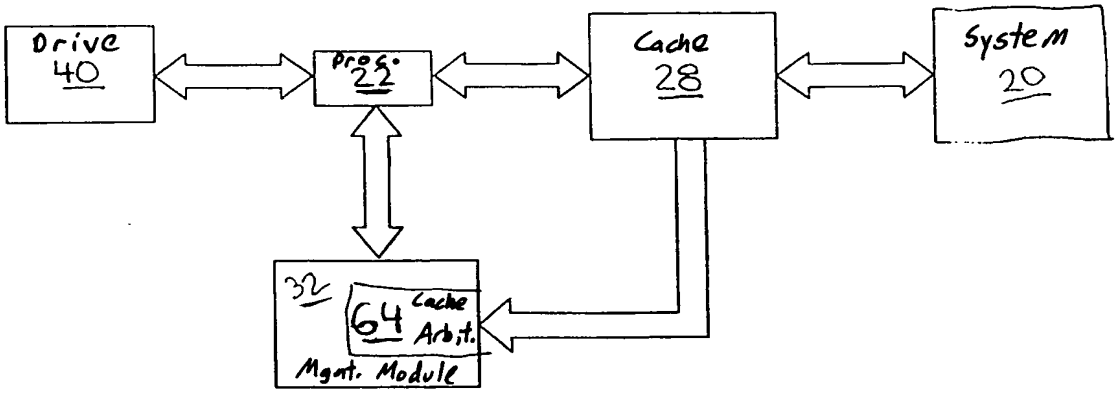

FIG. 5

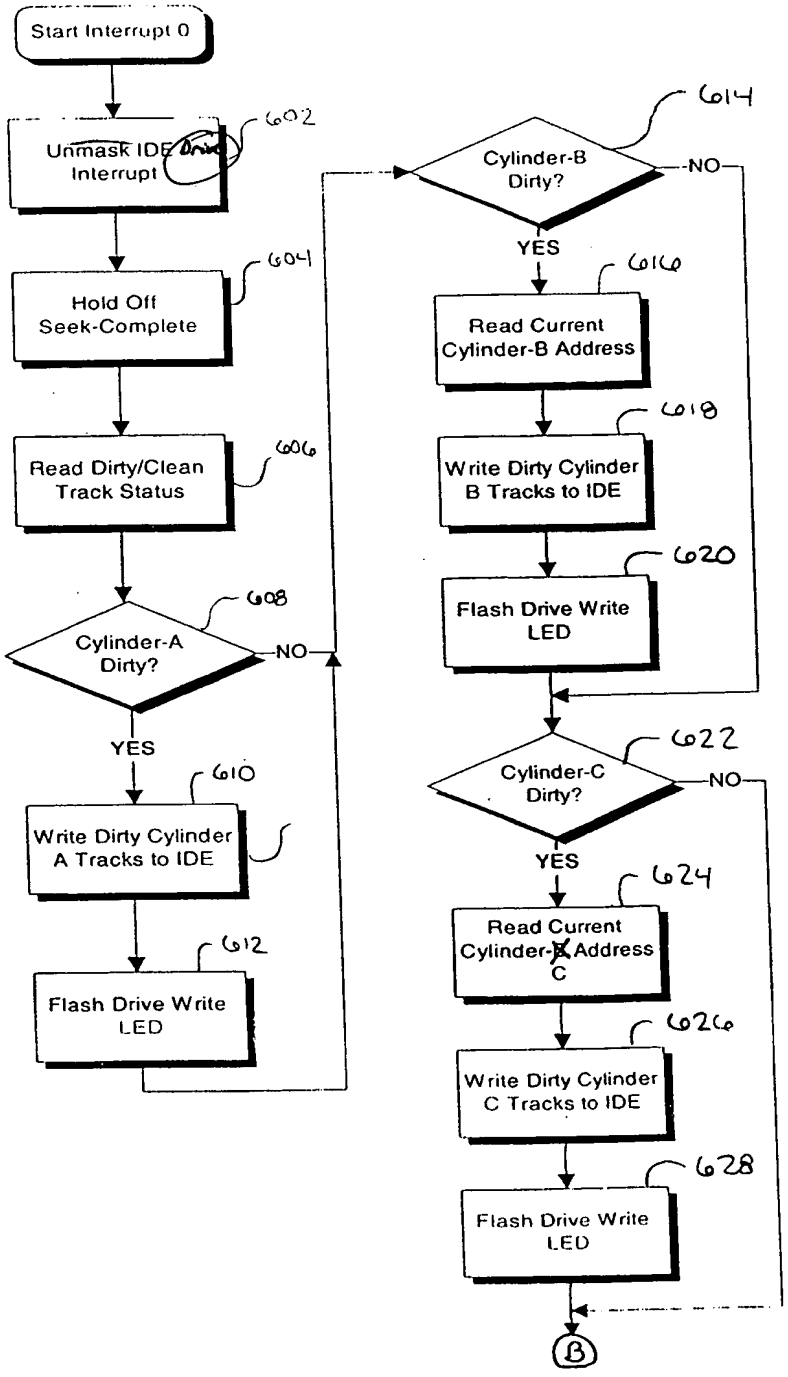

FIG. 6A

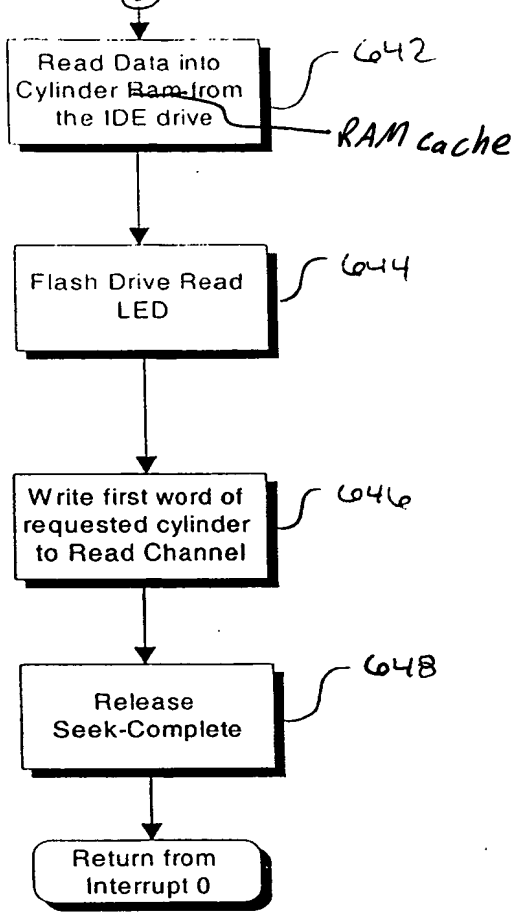

FIG. 6C

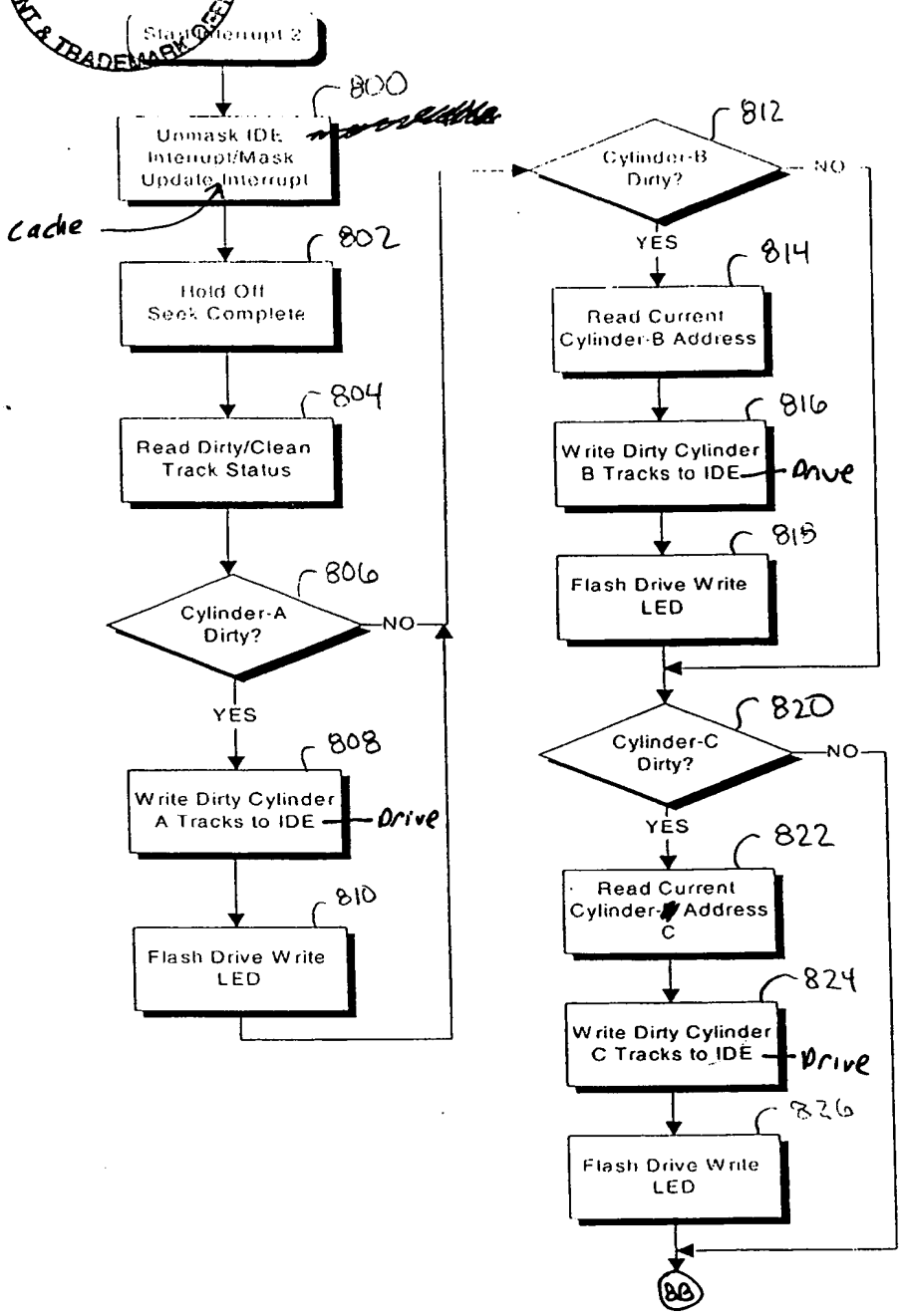

FIG. 8A

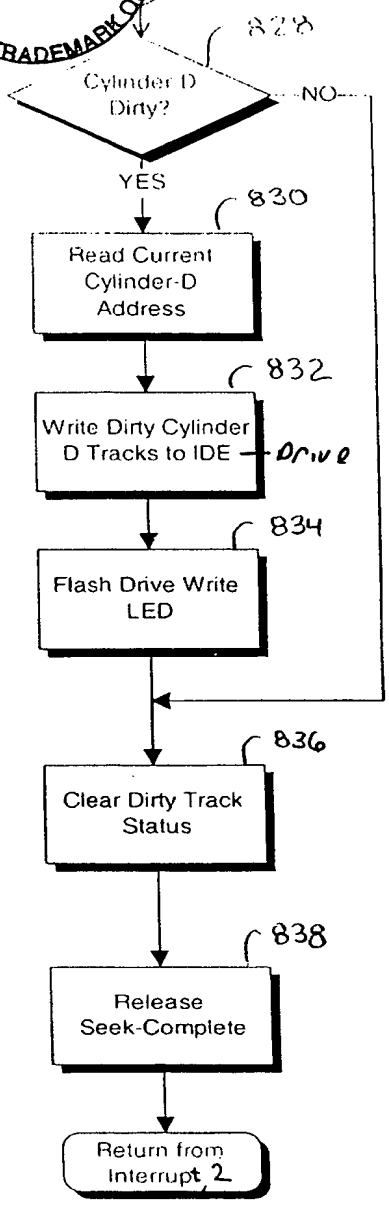

FIG. 8B

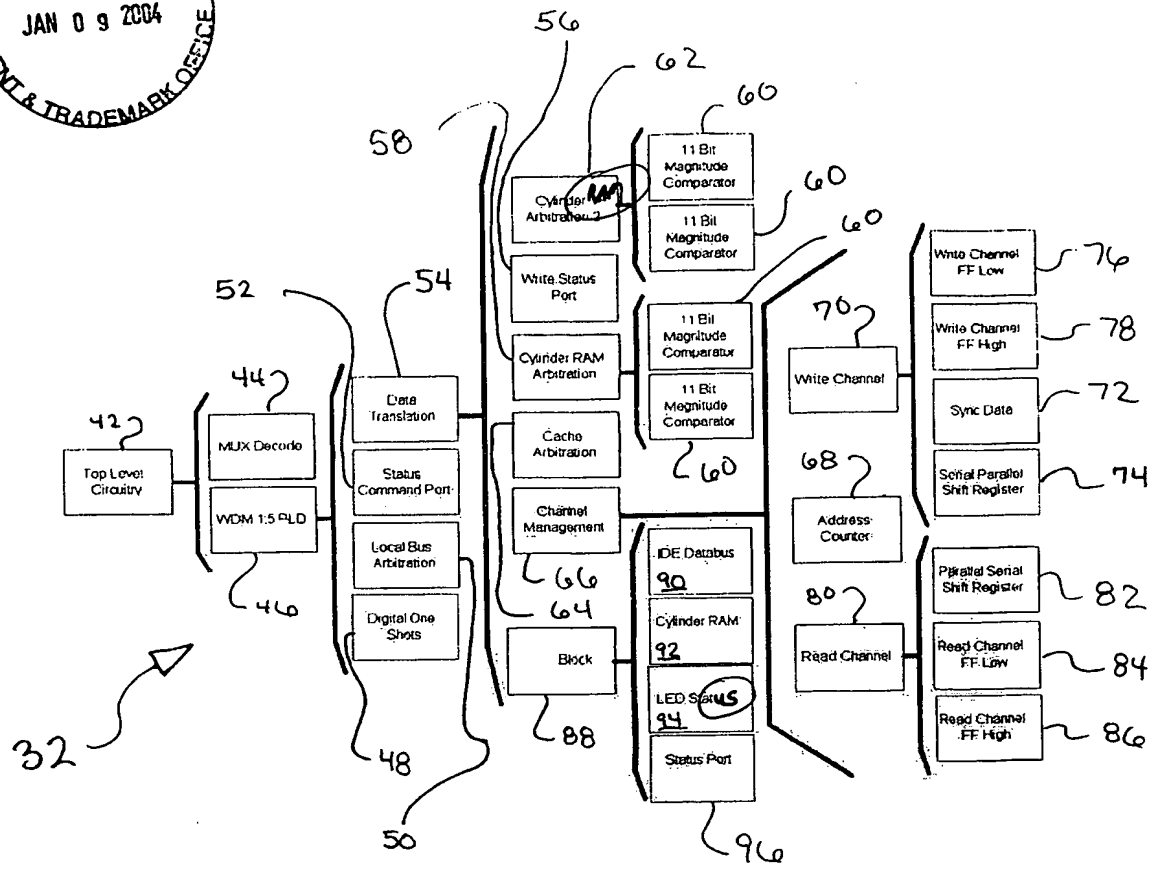

Fig. 9

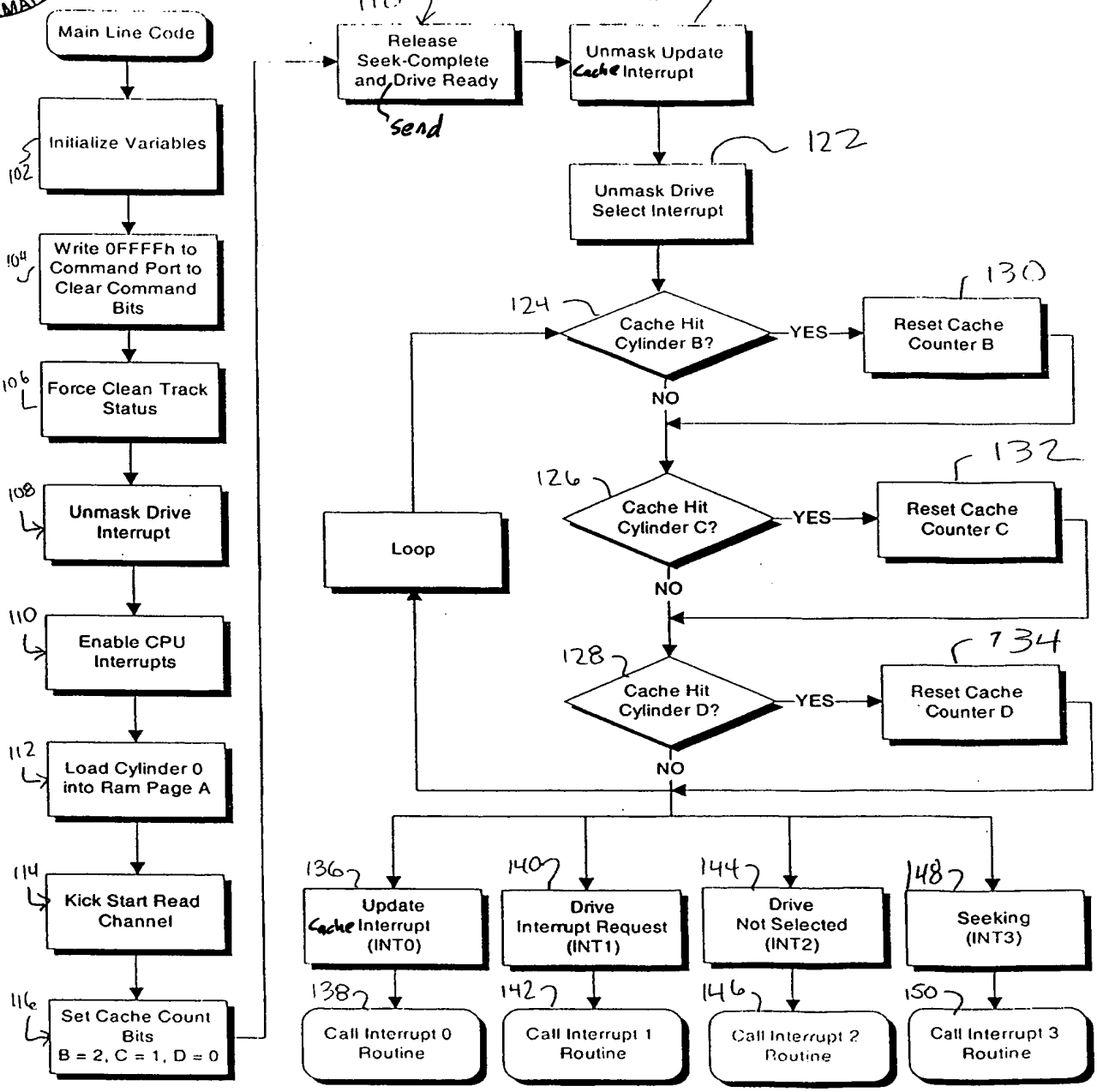

FIG. 10

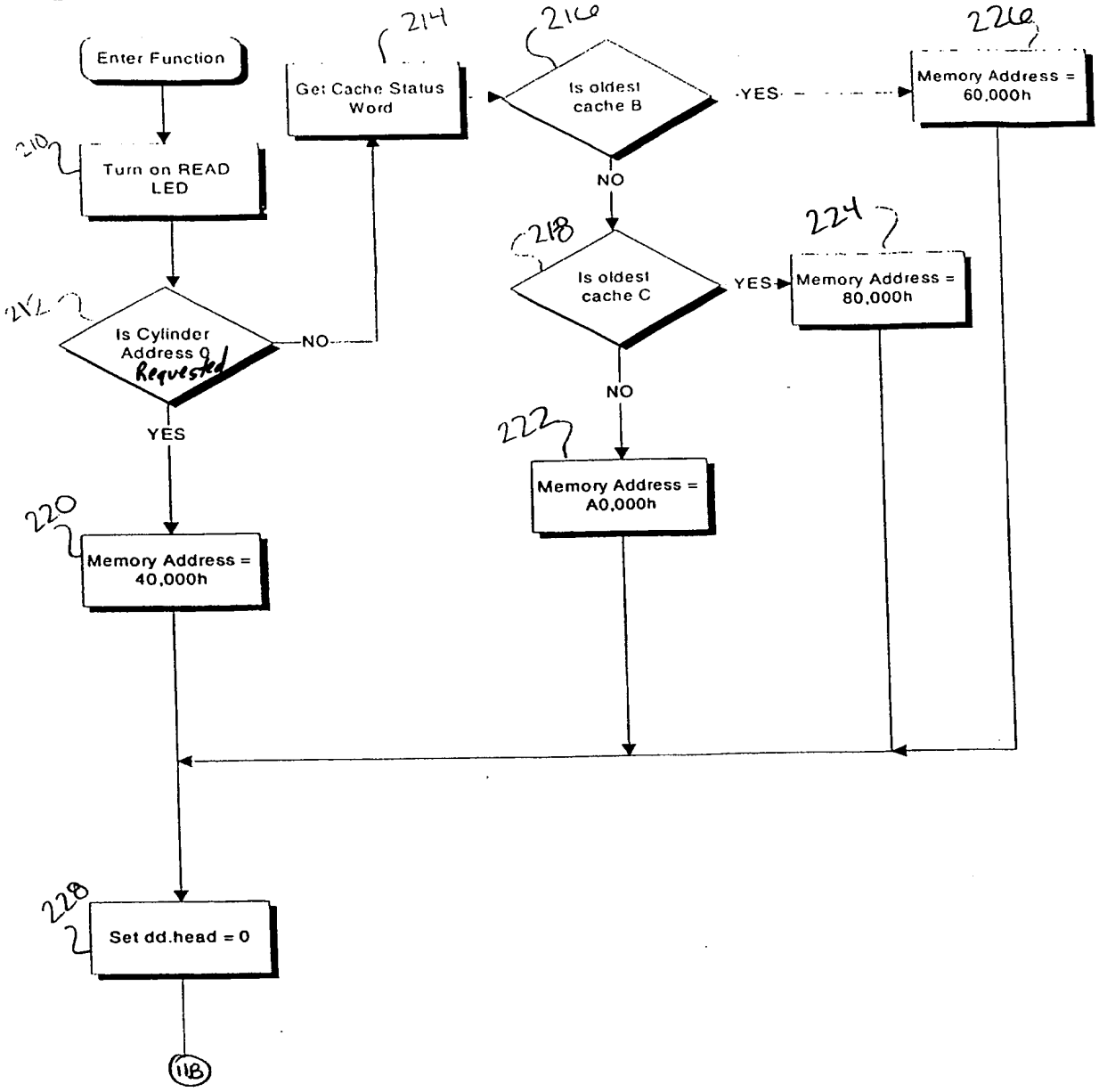

Fig. 11A

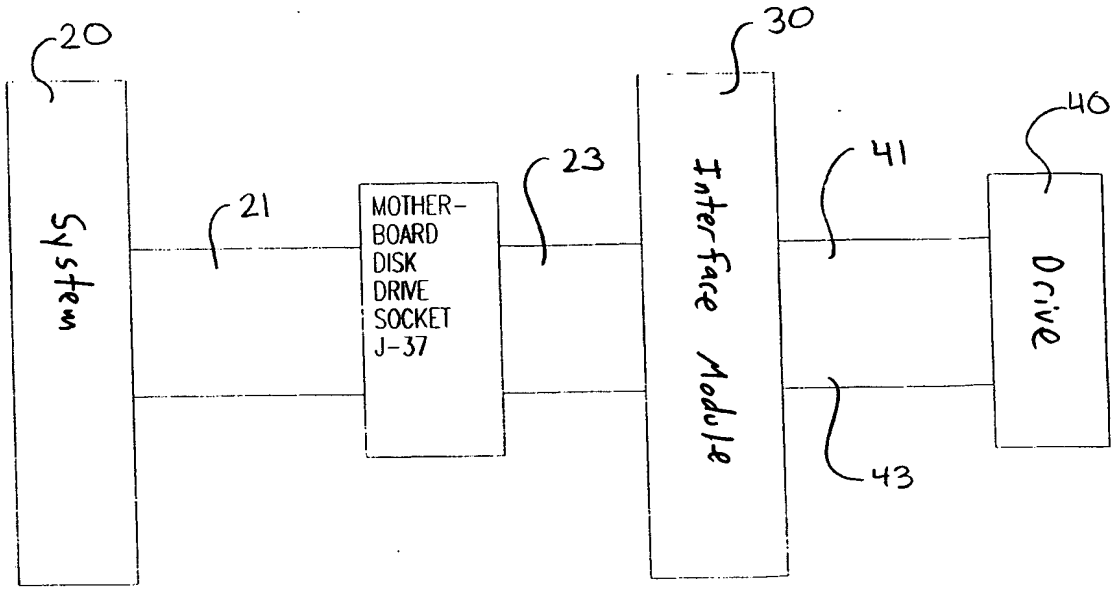

FIG. 13

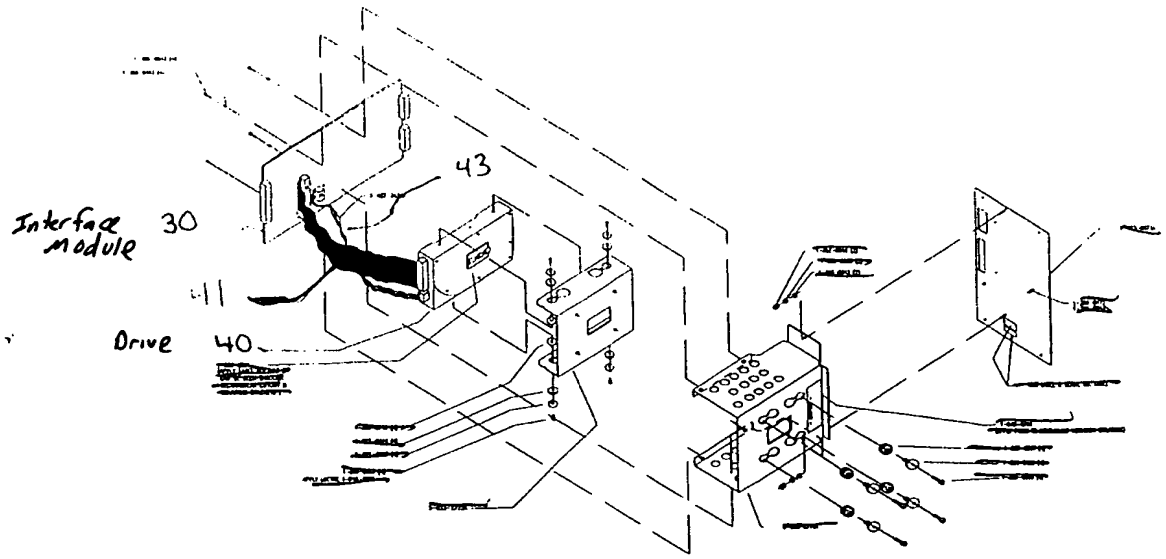

FIG. 14